Customer No. 22,852
Attorney Docket No. 03180.0357

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Hiroshi MATSUSHITA et al.	
	Group Art Unit: TBA
Application No.: Not Yet Assigned	
	Examiner: TBA
Filed: March 17, 2004	
For: METHOD FOR ANALYZING FAIL BIT MAPS OF WAFERS AND APPARATUS THEREFOR	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

The following is listed on the accompanying PTO-1449 and is in a non-English language. An English-language abstract is attached.

1. Japanese Patent Laid Open (Kokai) No. 2001-210097 - This document discloses a failure analyzing method using a fail bit count data.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the Office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: March 17, 2004

By: _____
Richard V. Burgujian
Reg. No. 31,744

Enclosures
RVB/FPD/cma

OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	03180.0357	Application No.	TBA
Applicant	Hiroshi MATSUSHITA et al.		
Filing Date	March 17, 2004	Group:	TBA

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		2001-210097	08/03/2001	Japan			Abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Copy of U.S. Patent Application for Hiroshi MATSUSHITA et al., Serial No. 10/107,297, filed March 28, 2002
	Copy of U.S. Patent Application for Hiroshi MATSUSHITA, Serial No. 10/608,155, filed June 30, 2003
	K. Mitsutake, et al., "New Method of Extraction of Systematic Failure Component", Proc. 10th Int. Symp. Semiconductor Manufacturing, pp. 247-250, (2001)
	M. Sugimoto et al., "Characterization Algorithm of Failure Distribution for LSI Yield Improvement", Proc. 10th Int. Symp. Semiconductor Manufacturing, pp. 275-278, (2001)
	K. Nakamae, et al., "Fail Pattern Classification and Analysis System of Memory Fail Bit Maps", Proc. 4th Int. Conf. Modeling and Simulation of Microsystems, pp. 598-601, (2001)

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce